APPENDIX A

Low-Cost Signature Testing of RF Circuits

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Abstract: *Production test costs for today's RF circuits are rapidly escalating. Two factors are primarily responsible for this cost escalation: (a) The high cost of RF ATE and (b) Long test times demanded by elaborate performance tests. In this paper, we propose a low-cost test approach for the test of RF circuits using modulation of a low frequency test signal and subsequent demodulation of the DUT response. The demodulated response of the DUT is used as a signature from which all the performance specifications are predicted. We believe the proposed low-cost solution can be easily built into a load board that can be interfaced to an inexpensive tester.*

1.0 Introduction

With the explosion in the wireless industry, RF integrated circuits are being used increasingly in a wide range of applications. Manufacturers of wireless applications are integrating RF, analog and digital blocks on the same silicon die for better performance and low cost. Production testing of high performance RF circuits is a major component of total RF electronics manufacturing cost because of elaborate tests and expensive testers. New RF test solutions are needed to keep pace with the phenomenal growth in the wireless industry, and the ever increasing consumer demand for products with higher functionality at low price.

Signature testing has been proposed as a low cost alternative to specification testing of analog circuits [1,2]. It has been shown that without explicitly testing for the circuit specifications, analog performance can be predicted by using the transient response of the DUT as a signature (hence the name *signature test*). This technique coupled with a systematic test optimization procedure enables robust testing while reducing test costs dramatically.

The use of modulated signals for the test of RF circuits has been well studied in the past [3]. Recently, a new technique called Modulated vector network analysis (MVNA) [4] has been proposed for making classic RF measurements on wideband modulated signals. Using modulated signals, the technique is capable of measuring S-parameters and performing signal analysis using a single data acquisition. Further, this technique allows the behavior of the wideband components to be tested close to their real-world operation.

In this paper, we propose a new signature testing approach [5] for testing RF circuits using test signal modulation and test response demodulation. The proposed approach involves the following steps:

1. The ATE supplies carefully designed baseband test stimulus to the loadboard.
2. On the load board, the test stimulus is modulated onto a carrier. This modulated carrier is the test input signal to the DUT.
3. DUT response is demodulated and baseband signal is sent back to the ATE.
4. The design of the test stimulus (baseband+carrier) is done in such a way that performance variations in DUT cause significant changes in the response seen by the ATE.

The emphasis of the proposed approach is to provide a highly cost-effective solution for production testing of RF circuits. The attractive features of our solution are (a) The modulator and demodulator can be easily built into the DUT loadboard and (b) The test signal applied to the loadboard and the signature response to be measured are both baseband, facilitating the use of a low cost ATE.

The rest of the paper is organized as follows. Section 2 describes the proposed approach for RF signature test and a procedure for test signal optimization. Section 3 discusses application of the proposed approach to the testing of a low noise amplifier (LNA) circuit. Section 4 concludes the paper.

2.0 Proposed Approach

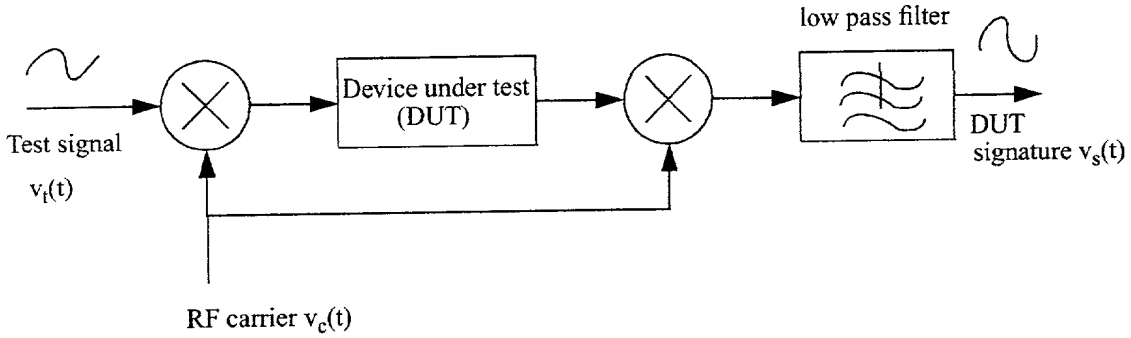


FIGURE 1. Signature testing of RF circuits

The proposed signature test approach is illustrated in Figure 1. A baseband test signal v_t is modulated on a high frequency carrier and is applied to the DUT. Output of the DUT is demodulated and filtered so that the resulting signature only has baseband variations. As the applied test signal $v_t(t)$ and the demodulated test response $v_d(t)$ are both baseband, the proposed test approach obviates the need for an expensive RF tester.

Further the modulator and demodulator can easily be designed into the loadboard, leading to an inexpensive test solution.

A regression model built between the DUT signature and the DUT measurements allows the prediction of DUT measurements without explicitly testing for them [1]. The process is illustrated in Figure 2. Several different DUT samples from the IC manufacturing process are considered and the DUT measurements are obtained using a high performance ATE. For each of these samples, an optimized baseband test signal is applied and the test signature is obtained by digitizing samples of the demodulated DUT response.

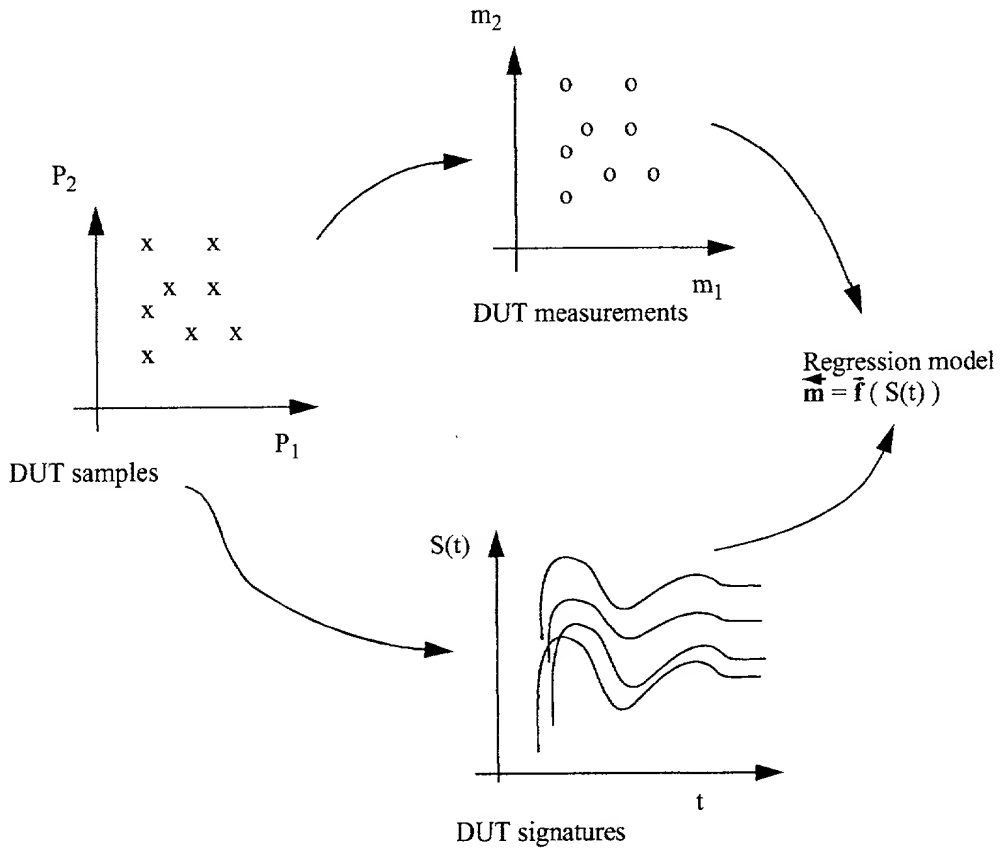


FIGURE 2. Relationship between DUT measurements and signature

The test signal applied to the DUT has to be chosen so as to minimize the error in predicting DUT measurements from the signature response. For this purpose, we use the optimization procedure described in [2]. More specifically, the prediction error for *ith* measurement, for a small perturbation in process parameters is given by

$$\sigma^2_{e(i)} = \sigma^2_{p(i)} + \sigma^2_{n(i)}$$

where σ_p is the least squared error between actual and predicted specifications for a small perturbation in (manufacturing) process parameters, and σ_n is the error contributed by measurement noise [2]. The objective function to be minimized is obtained as

$$F = \sum_{j=1,..,n} k_j \quad \text{where} \quad k_j = 1 + \frac{\left(1 - \frac{\sigma_{e(i)}}{\sigma^*}\right)}{n} \quad \text{for } \sigma_{ei} < \sigma^*$$

$$= \frac{\sigma_{e(i)}}{\sigma^*} \quad \text{for } \sigma_{ei} \geq \sigma^*$$

σ^* being the maximum allowed prediction error, and n the number of DUT measurements.

The resulting objective function is minimized using *genetic optimization* [6], where successive generations of a piecewise linear test stimulus (encoded as a genetic string) yield decreasing values of the objective function.

3.0 Experimental results

This section presents simulation results for a RF amplifier to illustrate the proposed approach. The application circuit is a 900 MHz low-noise amplifier (LNA) [7]. Figure 3 shows the schematic for the LNA. For illustration, three measurements were considered: Conversion gain, Noise Figure, and Third-order intercept point. Conversion gain and noise figure performances were measured at 900 MHz while the third-order intercept was measured by applying two input frequencies at 900 MHz and 920 MHz and observing the third-order harmonics at 880 MHz and 940MHz. The LNA circuit was simulated using the SpectreRF simulator [7]. SpectreRF analyses support efficient calculation of operating point, transfer function, noise and distortion of common RF and communication circuits. The DUT measurements were extracted using the Cadence Open Command Environment for Analysis (OCEAN) [8].

The objective of our test approach is to replace conventional DUT measurements (requiring an expensive RF ATE) with a signature test that can be applied using a low-cost ATE for production test of the DUT. The proposed signature test has to be effective throughout the range of variation expected in the manufacturing process of the DUT. For the circuit in Figure 3, the important process variations comprise of variation in the values of the resistors, capacitors and the BJT model parameters. For BJTs, the following model parameters were considered: saturation current (I_s), Forward current gain (β_f), Forward early voltage (V_{af}), base resistance (r_b), current corner for beta (i_{kf}). Other BJT parameters were found to have negli-

gible impact on the behavior of the LNA circuit. We further assume the parameter variations to be uniformly distributed around their nominal values.

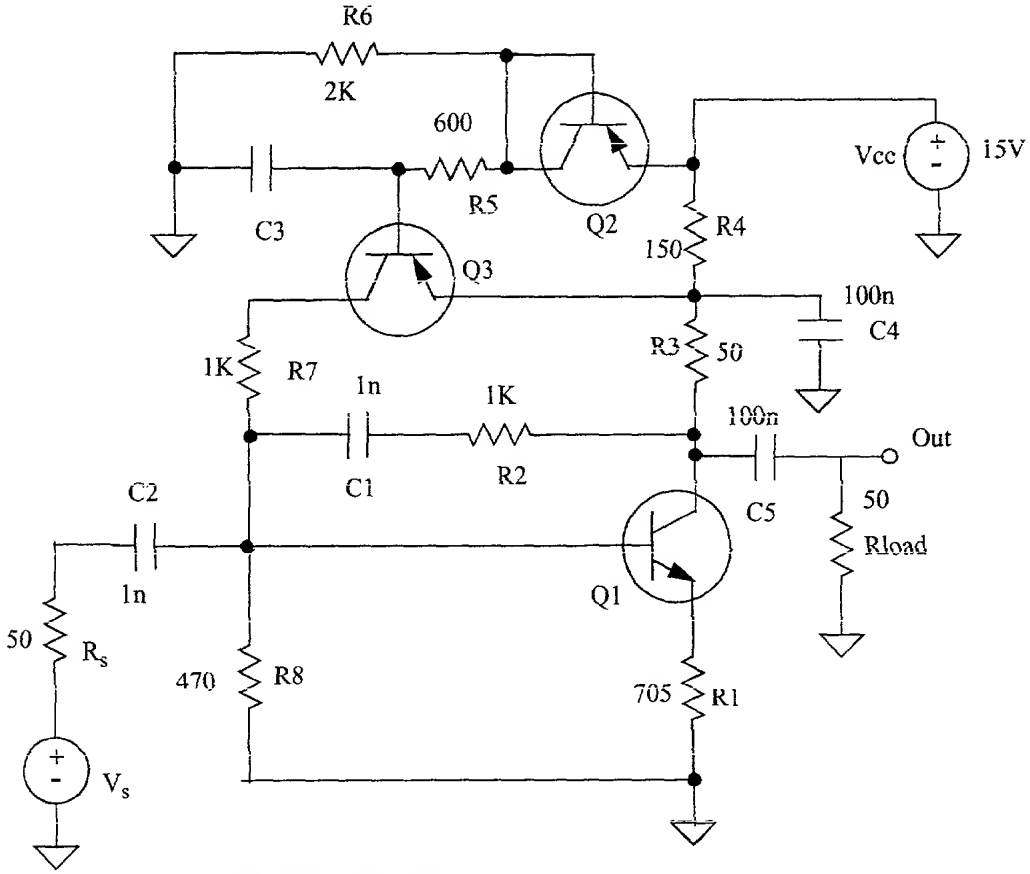


FIGURE 3. 900 MHz Low-noise amplifier

Following the ATPG approach described in Section 2, a linear prediction model is built to predict the LNA specifications from its signature response, obtained from Figure 1. For modulation and demodulation, a 10dBm, 900 MHz RF carrier is chosen. The demodulated DUT response is then passed through a low pass filter with a cutoff frequency of 10MHz. The DUT signature is obtained by sampling the filtered response at the nyquist rate (20MHz).

A genetic optimization algorithm is then used to synthesize a piecewise linear test stimulus for minimizing the least squared error between the actual and predicted specifications for a small perturbation in the process parameters. Further, to keep the simulation time short, the test signal is constrained to be of 5us duration. Figure 4 shows an optimized test stimulus after running 10 iterations of the genetic algorithm. Figure 5 shows the signature of 100 sample circuits in response to the applied test stimulus.

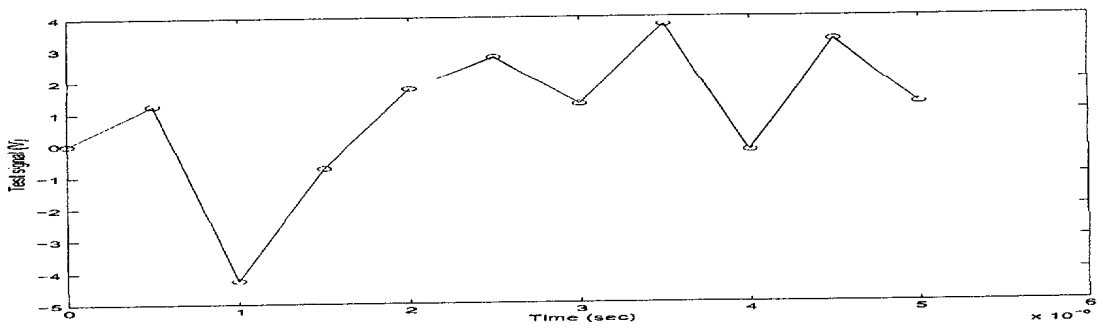


FIGURE 4. Optimized test stimulus

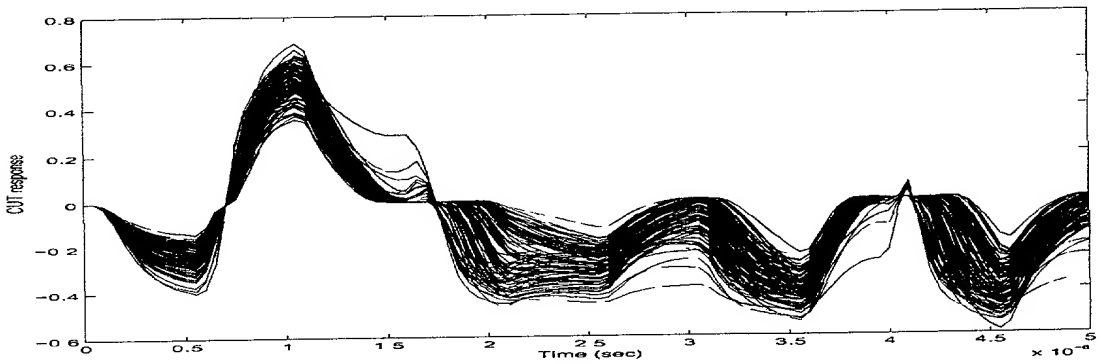
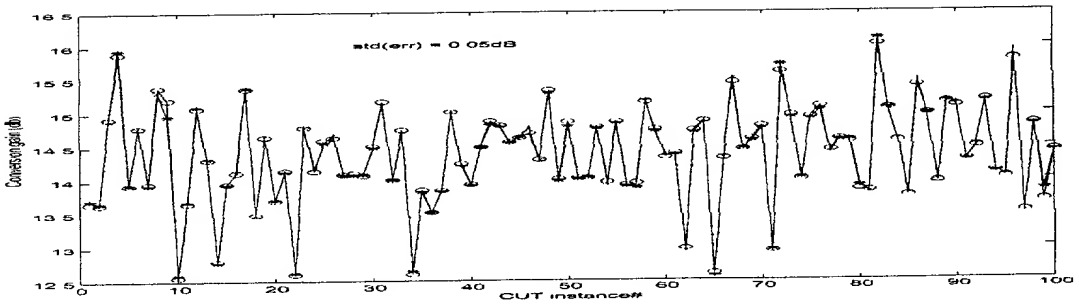
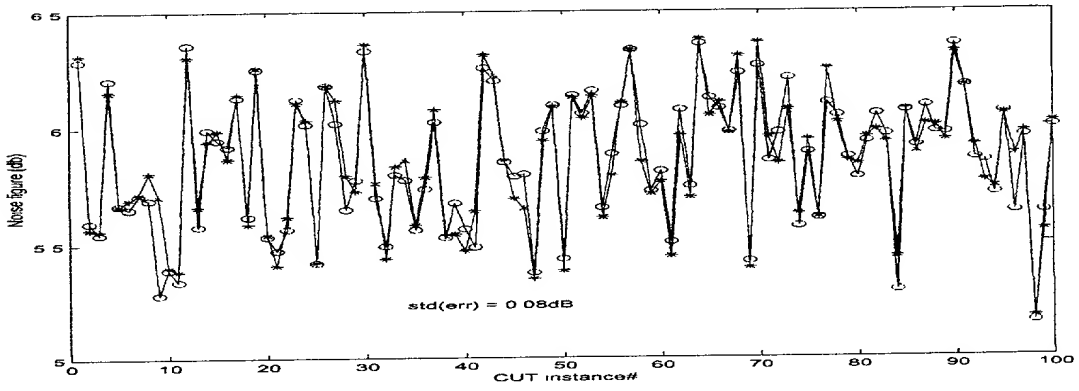


FIGURE 5. Signature response for 100 different circuit instances

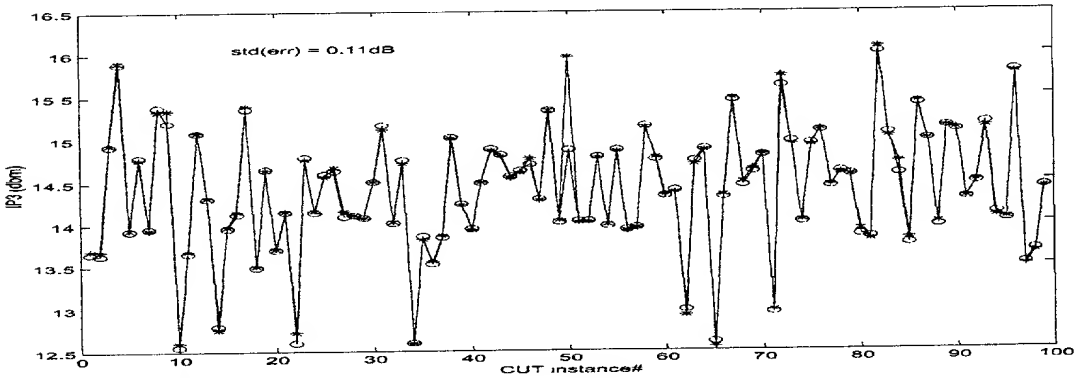
To validate the proposed signature test, we considered several circuit instances obtained by sampling the uniformly distributed process parameters. For correlation, a multivariate regression model was built between the DUT measurements (conversion gain, noise figure and IP3) and the signature responses for 200 circuit instances. Thereafter, DUT measurements for 100 more circuit instances were predicted from their signatures using the correlation model. Figure 6 shows the prediction results assuming a $\pm$ 25% uniform distribution for the process parameters. Measured values of conversion gain, noise figure and IP3 for the 100 circuit instances obtained by direct simulation are shown by a 'o' and those predicted by signature test are denoted by a '*'. The plots show an excellent agreement between direct measurements and those predicted using signature test. The attractive feature of our technique is that these results were obtained using an extremely short duration (5us) test signal, promising significant savings in test costs.



(a) Conversion gain



(b) Noise Figure

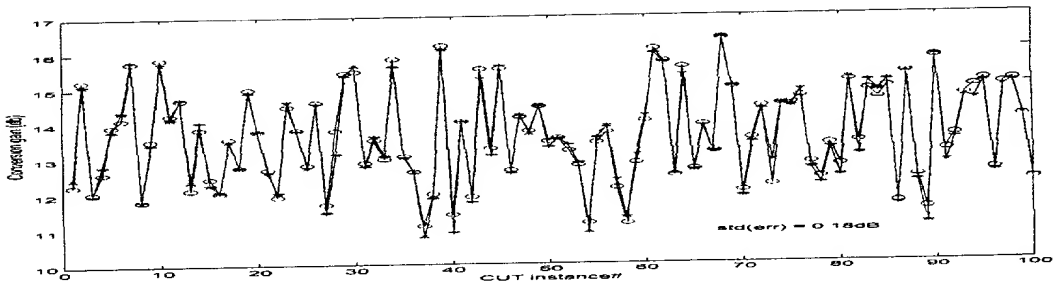


(c) Third-oder intercept

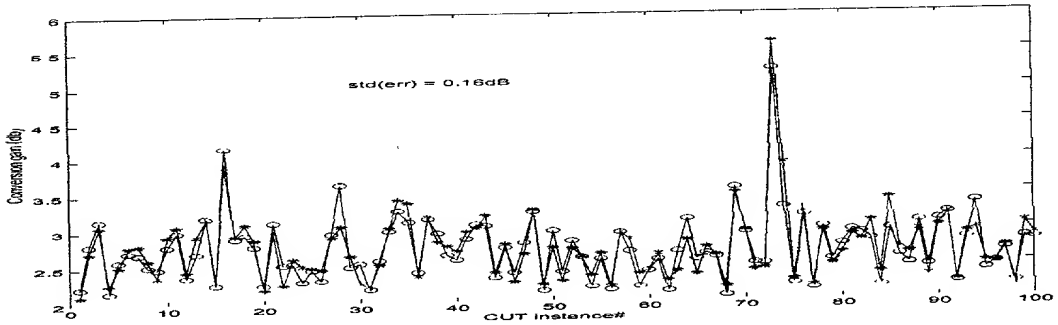
-o- Direct measurement
-*- Signature Test

FIGURE 6. Predicted and Actual DUT measurements with +/- 25% component variations

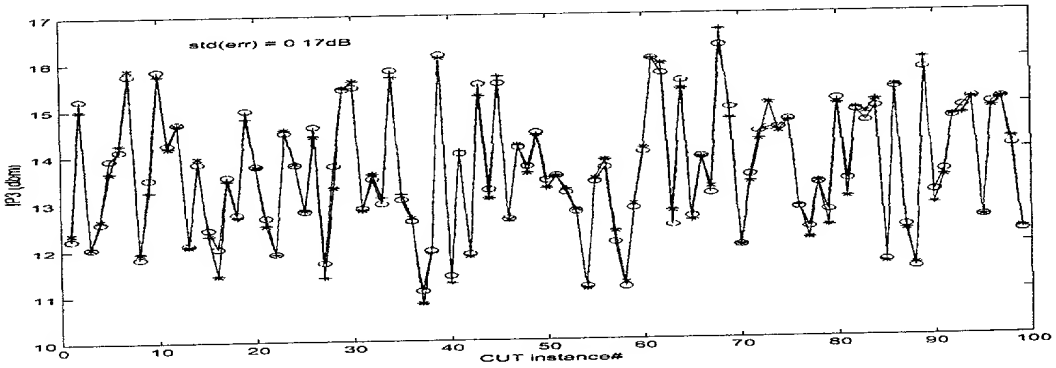
Figure 7 shows similar plots for a wider (± 50%) process distribution. In reality, most modern IC manufacturing processes are more tightly controlled. The results suggest that even for IC fabs with wide process spreads, the proposed signature test technique holds considerable promise.



(a) Conversion gain



(b) Noise Figure

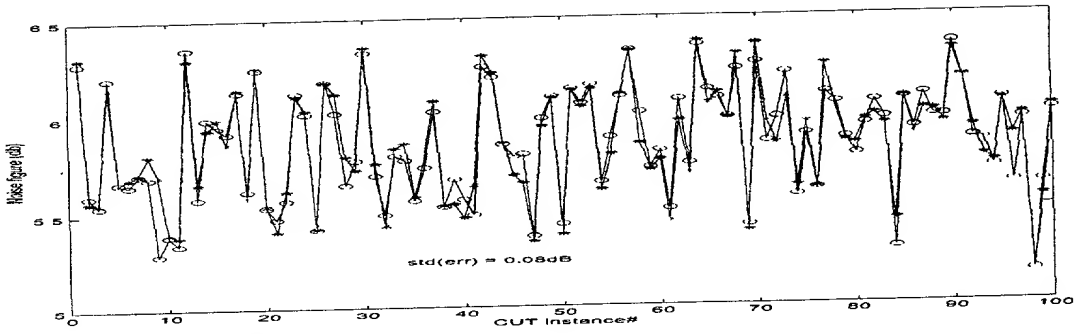


(c) Third-oder intercept

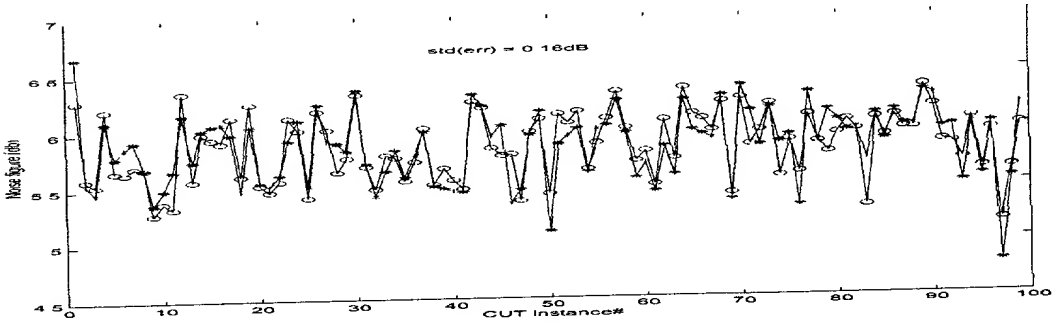
-o- Direct measurement
-*- Signature test

FIGURE 7. Predicted and Actual DUT measurements with +/- 50% component variations

Figure 8 depicts the impact of noise when measuring signature response. The plots show signature test results for noise figure measurements when additive gaussian noise is added to the signature response of the DUT. It can be seen from the results that there is a close agreement between the actual and predicted values of noise figure even with a large (5mv RMS) measurement noise. The experiment suggests that robust signature test performance is possible in the presence of measurement noise.



(a) Zero additive noise



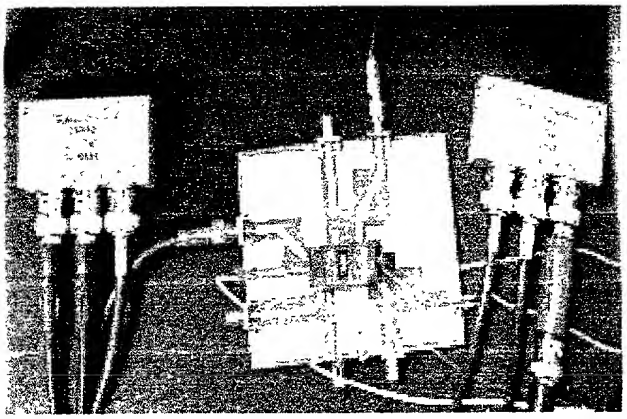
(b) 5mV (rms) additive gaussian noise

-o- Direct measurement
-*- Signature test

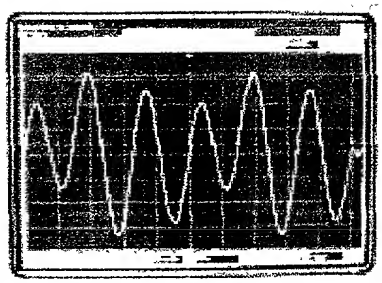
FIGURE 8. Effect of additive noise on signature test results

3.1 Hardware Validation

For hardware validation of the proposed approach, we built a RF frontend module using a RF2401 monolithic integrated receiver front-end IC from RF MicroDevices. The mixer and lowpass filter modules for generating signature test were obtained from Mini-Circuits. Figure 9a. shows a picture of the signature test prototype. The DUT signature obtained in response to a sinewave test (500 mV p-p, 2MHz) is shown in Figure 9b. We are currently making measurements on several frontend IC samples from RF MicroDevices. We hope to include data from these experiments in the final version of the paper.



(a) RF Frontend



(b) Signature response

FIGURE 9. RF signature test hardware prototype

4.0 Conclusions

In this paper, we proposed a low-cost technique for the signature testing of RF circuits. The proposed solution can be easily built into a load board that can be interfaced to an inexpensive tester. As the DUT measurements are obtained on a low-cost ATE using an extremely short duration test stimulus, significant savings in production test costs of RF circuits is made possible.

5.0 References

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